

 **EEL 4744**  
EEL 4744C: µP Apps

## Menu

- General-Purpose Input/Output (GPIO) on the XMEGA
- Port Remapping



 See examples on web-site:  
[doc8331](#), [doc8385](#),  
[GPIO\\_Output.asm](#)

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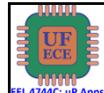
## XMEGA GPIO Overview

See [doc8385](#),  
Section 15

- GPIO multiplexing (MUX) registers are used to select the operation of shared pins
  - > Pins are named by their general purpose I/O name
  - > All functions are individual per pin, but several pins may be configured in a single operation
  - > All ports have true Read-Modify-Write (RMW) functionality when used as general purpose I/O ports
  - > The direction of one port pin can be changed **without** unintentionally changing the direction of any other pin
  - > Output port pins can be configured as wired AND or Wire-OR (see [doc8385](#), section 15.3.5)

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**GPIO Ports**

- The following are available ports
  - >PORTA, PORTB, PORTC, PORTD, PORTE, PORTF, PORTH, PORTJ, PORTK, PORTQ, PORTR
- Most port pins have alternate pin functions in addition to being a general purpose I/O pin
- When an alternate function is enabled, it might override the normal port pin function or pin value
- See doc8385, section 33 for alternate pin functions
  - >For example, ALE (address latch enable) signals use Port H pins (see Table 33-7) **See doc8385, Section 33**
    - We'll see this in **Lecture 09: Address & Data bus timing & Interfacing**

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**See doc8331,  
Section 13**

**See doc8385,  
Section 15**

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## Setting XMEGA GPIO Pins

- Each port has one Data Direction (**DIR**), Data Output Value (**OUT**), and Data Input Value (**IN**)
- Direction of the pin is decided by the DIRn bit in the DIR register.
  - >If 1 written to DIRn, pin n is output, OUTn sets pin n value to high
  - >If 0 written to DIRn, pin n is input, OUTn sets pin n value to low
  - >The IN register is used for reading the pin value
  - >I/O pins are tri-stated when reset condition becomes active, even if no clocks are running

**See doc8331,  
Section 13.2**

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## EEL 4744 Port Direction Descriptions

- The following Port registers are available

([OPEN the manual](#): doc8331, Sec 13.13)

See doc8331,  
Section 13.13

**>DIR** – Data Direction register

- If a one is written to DIRn, pin n is configured as an output pin
- If a zero is written to DIRn, pin n is configured as an input pin

**>DIRSET** – Data Direction Set Register

- Writing a one to a bit will set the corresponding bit in DIR
- Reading will return the value of the DIR register

**>DIRCLR** – Data Direction Clear Register

- Writing a one to a bit will clear the corresponding bit in DIR
- Reading will return the value of the DIR register

**>DIRTGL** – Data Direction Toggle register

- Writing a one to a bit will toggle the corresponding bit in DIR
- Reading will return the value of the DIR register



## EEL 4744 Port Output Descriptions

- The following **port registers** are available

**>OUT** – Data Output Value

- Sets the data output value for the individual pins of the port
- If a one is written to OUTn, pin n is driven high
- If a zero is written to OUTn, pin n is driven low
- For this to have any effect, the pin direction must be output

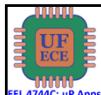
**>OUTSET** – Data Output Value Set register

- If a **one** is written to bit n, OUTn is set; writing a 0 has no affect
- Reading this register will return the value in the OUT register

**>OUTCLR** – Data Output Value Clear register

- If a **one** is written to bit n, OUTn is cleared
  - Writing a zero has no affect
- Reading this register will return the value in the OUT register

See doc8331,  
Section 13.13

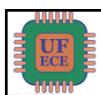
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## Port Output/Input Descriptions

- The following Port registers are available
  - >**OUTTGL** – Data Output Value Toggle register
    - If a **one** is written to bit n, OUTn will toggle; writing a zero has no affect
    - Reading this register will return the value in the OUT register
  - >**IN** – Data Input Value register
    - INn shows the value of pin n
    - The input is not sampled and cannot be read if the digital input buffers are disabled
- See doc8331, section 13.13.10 for the following
  - INTCTRL – Interrupt Control reg, INT0MASK – Interrupt 0 Mask reg,
  - INT1MASK – Interrupt 1 Mask reg, INTFLAGS – Interrupt Flag reg, ...

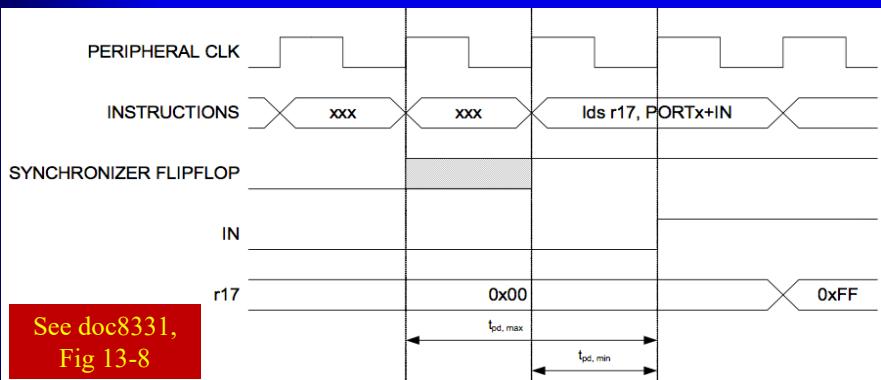
See doc8331,  
Section 13.13

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## XMEGA: Reading the I/O pin

- Independent of the pin data direction, the pin value can be read from the IN register
- If the digital input is disabled, the pin value cannot be read
- $t_{pd,max}$  and  $t_{pd,min}$  are max and min propagation delays



See doc8331,  
Fig 13-8

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### Example with GPIO\_Output

- Simulate **GPIO\_Output**
  - In **I/O (Debug | Windows | I/O)** in the **Filter:** box type “**portd**” then return
  - Select the **I/O Port Configuration (PORTD)**
  - Look at DIR through OUTTGL as code is run
  - While running the simulator, look at the **Disassembly** file
    - One quick way to see the address for the instructions: **Debug | Windows | Disassembly** (or use Alt-8)
      - Go to address 0x0 (for program memory) and 0x100 for program
    - Look at the list file (.lss) when not running under **Output Files**
- > Emulate **GPIO\_Output** and repeat above with the uPAD
  - Watch the PortD lights blink

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## EEL 4744

### Switch and LED Circuits

- See *Hardware: Getting Started* on our Classes webpage (as well as the 3701 website under Software/Docs)
  - > Switch Circuits
  - > LED Circuits

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See doc8331,  
Sec 13.13.14

## Port Remapping for µPAD's RGB LEDs

- µPAD RGB LEDs on PD4, 5, and 6, respectively.
  - > If use time/counter (coming soon), may want to remap these as described below (see HW 2).
  - > **Bit 3 – TC0D: Timer/Counter 0 Output Compare D**
    - Setting this bit will move the location of OC0D from Px3 to Px7.
  - > **Bit 2 – TC0C: Timer/Counter 0 Output Compare C**
    - Setting this bit will move the location of OC0C from Px2 to Px6.
  - > **Bit 1 – TC0B: Timer/Counter 0 Output Compare B**
    - Setting this bit will move the location of OC0B from Px1 to Px5.
  - > **Bit 0 – TC0A: Timer/Counter 0 Output Compare A**
    - Setting this bit will move the location of OC0A from Px0 to Px4.

Bit	7	6	5	4	3	2	1	0
+0x0E	–	–	SPI	USART0	TC0D	TC0C	TC0B	TC0A
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

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# *The End!*

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